REMARKS

Claims 1-7 and 9-21 are pending in the present application. Claims 11, 16 and 17 have been amended.

Claim Rejections-35 U.S.C. 103

Claims 11-14 and 16-20 have been rejected under 35 U.S.C. 103(a) as being unpatentable over the Arase reference (Japanese Patent Publication No. 4-69939) in view of the Williams reference (U.S. Patent No. 5,998,837). This rejection is respectfully traversed for the following reasons.

The semiconductor device of claim 11 includes in combination a silicon substrate; an impurity region "of a first conductivity type formed in the silicon substrate, the impurity region having only an upper surface thereof exposed from the silicon substrate"; a first insulating film "formed on the silicon substrate, the first insulating film including a first opening over the upper surface of the impurity region"; a polysilicon plug "of a second conductivity type formed in the first opening in contact with the impurity region and on an upper surface of the first insulating film"; a second insulating film "formed on the polysilicon plug and on the upper surface of the first insulating film, the second insulating film having a second opening over the polysilicon plug"; and a conductive wiring layer "formed in the second opening in contact with the polysilicon plug and on an upper surface of the second insulating film". Applicant respectfully submits that the prior art as relied upon by the Examiner does not make obvious these

features.

The Examiner has primarily relied upon Fig. 1 of the Arase reference as disclosing the features of claim 11. However, Fig. 1 of the Arase reference merely illustrates what appears to be a p^+ type polysilicon plug 17a formed in an opening through an insulating layer and as in contact with n^+ type drain diffusion region 13, and aluminum film 18 as formed in contact with polysilcion plug 17a and on the insulating layer.

The structure in Fig. 1 of the Arase reference as relied upon by the Examiner does not include a second insulating film as formed on polysilicon plug 17a and on an upper surface of the corresponding insulating film illustrated in Fig. 1, and does not include a second insulating film as having a second opening over polysilicon plug 17a, as would be necessary to meet the features of claim 11. The structure in Fig. 1 of the Arase reference as relied upon by the Examiner does not include aluminum wiring 18 as formed in a second opening of a second insulating film so as to be in contact with polysilicon plug 17a and so as to be on an upper surface of a second insulating film, as would be necessary to meet the further features of claim 11.

That is, the Examiner has not established how the Arase reference may be interpreted as including a second insulating film formed on a polysilicon plug, a second opening in a second insulating film, and a conductive wiring layer as formed in a second opening of a second insulating film, as would be necessary to meet the features of claim 11. Since the prior art as relied upon by the Examiner fails

to meet all the features of claim 11, Applicant respectfully submits that this rejection of claims 11-14 and 16 is improper for at least these reasons.

With further regard to this rejection, the Examiner has secondarily relied upon the Williams reference. However, the manner in which the Williams reference has been relied upon to reject claim 11 is unclear. Particularly, on page 2 of the current Office Action dated May 19, 2005, the Examiner has acknowledged that the Arase reference "fails to disclose the required doping densities". In order to overcome this acknowledged deficiency of the Arase reference, the Examiner has alleged that the Williams reference "discloses a trench-gated power MOSFET with protective diode having adjustable breakdown voltage where in Claim 14 the required doping density is disclosed". The Examiner has alleged that it would have been obvious to include the required doping density in the Arase reference as taught by the Williams reference "in order to have a semiconductor device with increase reliability".

Applicant initially emphasizes that claim 11 as pending does not feature doping densities. It is thus unclear how the Williams reference has been relied upon to reject claim 11.

Moreover, the Examiner has apparently relied upon claim 14 of the Williams reference, which features "said third region is doped to substantially the same dopant concentration of said body region". (Applicant presumes that claim 14 of the Williams reference is dependent on claim 12 thereof, so as to provide antecedent for said third region.) However, the body region of the MOSFET of claim 14 of the Williams

reference, as dependent on claim 12, is featured as having second conductivity type, and the third region of claim 14 of the Williams reference is also featured as having second conductivity type and as being part of the at least one diode cell.

Claim 14 of the Williams reference thus presumably features that the second conductivity type body region of the MOSFET has the same dopant concentration as the second conductivity type third region of the at least one diode cell. Claim 14 of the Williams reference does not feature that an impurity concentration of an impurity region having a first conductivity type is substantially equal to an impurity concentration of a polysilicon plug having a second conductivity type, whereby the polysilicon plug is formed in a first opening of a first insulating film. Accordingly, even though the Examiner's reliance upon the Williams reference is unclear, the Williams reference does not appear to make obvious the features as asserted by the Examiner. Applicant therefore respectfully submits that the semiconductor device of claim 14 would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together, and that this rejection of claim 14 of the present application is improper for at least these additional reasons.

The semiconductor device of claim 17 includes in combination a first insulating film "formed on the silicon substrate, the first insulating film including a first opening over the upper surface of the impurity region"; a polysilicon plug "of a second conductivity type formed in the first opening in contact with the impurity region"; a second insulating film "formed on an upper surface of the first insulating film, the

second insulating film having a second opening over the polysilicon plug"; and a conductive wiring layer "formed in the second opening in contact with the polysilicon plug and on an upper surface of the second insulating film".

Applicant respectfully submits that the semiconductor device of claim 17 would not have been obvious in view of the prior art as relied upon by the Examiner for at least somewhat similar reasons as set forth above. The Arase reference as relied upon by the Examiner does not disclose a second insulating film on an upper surface of a first insulating film, whereby the second insulating film has a second opening over a polysilicon plug. Consequently, the Arase reference also fails to disclose a conductive wiring layer formed in a second opening in a second insulating film, as would be necessary to meet the features of claim 17.

Moreover, even though the Examiner's reliance upon the Williams reference is unclear, the Williams reference does not appear to make obvious the features as asserted by the Examiner. Applicant therefore respectfully submits that the semiconductor device of claim 20 would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together, and that this rejection of claims 17-20 is improper for at least these reasons.

Allowable Subject Matter

Applicant respectfully notes the Examiner's acknowledgment that claims 1-7, 9

and 10 are allowed.

Applicant also respectfully notes the Examiner's acknowledgement that claims 15 and 21 would be allowable if rewritten in independent form. Applicant however respectfully notes that independent claims 11 and 17 distinguish over and would not have been obvious in view of the prior art as relied upon by the Examiner for at least the reasons as set forth above, and that amendment of claims 15 and 21 to be in independent form is therefore unnecessary.

Conclusion

Applicant respectfully submits that claims 11, 16 and 17 have been amended merely to correct minor typographical errors. Accordingly, these above noted amendments should not be construed as narrowing scope within the meaning of *Festo*.

The Examiner is respectfully requested to reconsider and withdraw the corresponding rejection, and to pass the claims of the present application to issue, for at least the above reasons.

In the event that there are any outstanding matters remaining in the present application, please contact Andrew J. Telesz, Jr. (Reg. No. 33,581) at (571) 283-0720 in the Washington, D.C. area, to discuss these matters.

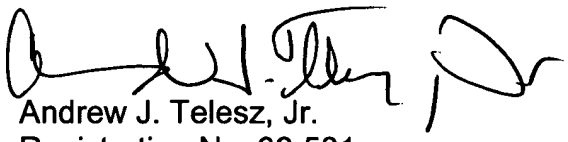
Pursuant to the provisions of 37 C.F.R. 1.17 and 1.136(a), the Applicant hereby petitions for an extension of one (1) month to September 19, 2005, for the period in which to file a response to the outstanding Office Action. The required fee of $120.00

should be charged to Deposit Account No. 50-0238.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment for any additional fees that may be required, or credit any overpayment, to Deposit Account No. 50-0238.

Respectfully submitted,

VOLENTINE FRANCOS & WHITT, P.L.L.C.



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